

ABSTRACT OF THE DISCLOSURE

A data memory circuit having divided several cache lines storing data, and several entries, and a tag circuit, are provided. The tag circuit having an array  
5 of an associative memory including a memory cell circuit having several memory cells storing address corresponding to the data stored in the data memory circuit and divided several rows, and a comparator circuit comparing the address stored in the memory cell  
10 circuit with input address, the comparator circuit comparing the address stored in divided several rows of the memory cell circuit with the input address concurrently in each of divided rows storing the address, and generating a cache hit/miss determination  
15 signal based on the comparative result of each row, the hit/miss determination signal being supplied to the data memory circuit.